**Laboratory Report Cover Sheet**

| SRM INSTITUTE OF SCIENCE AND TECHNOLOGY  Faculty of Engineering and Technology  Department of Electronics and Communication Engineering |
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| **18ECC103J Digital Electronic Principles**  **III Semester, 2021-2022 (ODD Semester)** |

**Title of Mini Project: Synchronous Timer**

**Date of Submission: 08/02/2022**

| **Particulars** | **Max. Marks** | **Marks Obtained** | | |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **Name:**  **Prem Sagar** | **Name:**  **Ganni Likhit** | **Name:**  **Kunal Keshan** | **Name:**  **Vaibhav Mohla** |
|  |  | **Register No.**  **RA2011004010039** | **Register No.**  **RA2011004010048** | **Register No.**  **RA2011004010051** | **Register No.**  **RA2011004010052** |
| Design | 20 |  |  |  |  |
| Demo verification &viva | 15 |  |  |  |  |
| Project Report | 05 |  |  |  |  |
| **Total** | **40** |  |  |  |  |

**REPORT VERIFICATION**

**Staff Name: Selvakumar J**

**Signature:**

**Objective:**

To design a synchronous timer using JK flip-flop.

**Software Used:**

Logisim.

**Components used:**

i) JK Flip-flop

ii) Clock

iii) Power source

iv) NOT Gate

v) AND Gate

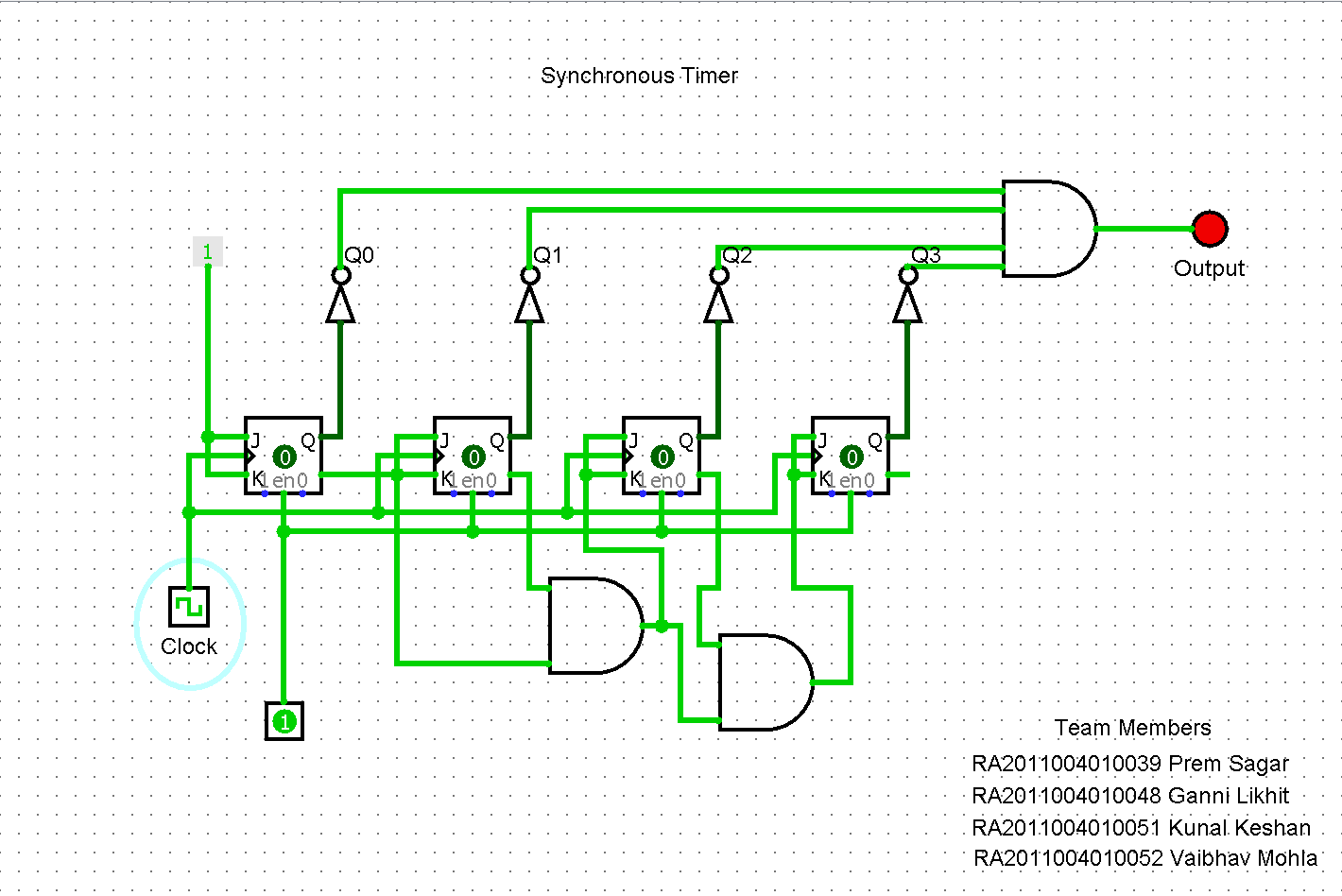
vi) LED

**Introduction:**

In this project, we will use a Down counter which will count the numbers in decreasing order. This will decrease its count. So inputs of the JK flip- flop are connected to the inverted Q (Q’). The 4 bit down counter is designed by using JK flip flop. The same external clock pulse is connected to all the flip flops.

As the counter has to count down the sequence, initially all the inputs will be in the high state as they have to count down the sequence. It will start with 1111 and end with 0000.

In the down counter, it should be remembered that the preceding flip flop will toggles only if the front flip flop produces low logic at its output.

**Circuit diagram:**

**Operation:**

In the down counter the 4-bit binary sequence starts from 1111 and decrements to 0000. Before understanding the working of the above down counter circuit, we should know about the [JK Flip flop.](https://www.electronicshub.org/jk-flipflop/)

In the above circuit, the two inputs of the flip flop are wired together. So , there are only two possible conditions that can occur, that is, either the two inputs are high or low.

If the two inputs are high then JK flip-flop toggles and if both are low JK flip flop remembers i.e. it stays in the previous state.

Let us see the operation. Here the clock pulse indicates an edge-triggered clock pulse.

1.) In the first clock pulse, the outputs of all the flip flops will be at 1111.

2.)In the second clock pulse, as inputs of J and k are connected to the logic high, the output of JK flip flop(FF0) changes its state. Thus the output of the first flip-flop(FF0) changes its state for every clock pulse. This can be observed in the above shown sequence. The LSB changes its state alternatively. Thus producing -0001

3.) In the third clock pulse, the next flip flop (FF1) will receive its J K inputs i.e (logic high) and it changes its state. At this state, FF0 will change its state to 0. And thus input on the FF1 is 0. Hence the output is -0010

4.) Similarly, in the fourth clock pulse, FF1 will not change its state as its inputs are in low state, it remains in its previous state. Though it produces the output to FF2, it will not change its state due to the presence of AND gate. FF0 will again toggle its output to logic high state. Thus Output is 0011.

5.) In the fifth clock pulse, FF2 receives the inputs and changes its state. FF0 will have low logic on its output and FF1 will also be low state producing 0100.

**Result:**

If the outputs (Qo, Q1, Q2, Q3) are zero then the LED will glow.

**Conclusion:**

By this mini project we learnt how to design Synchronous Timer.